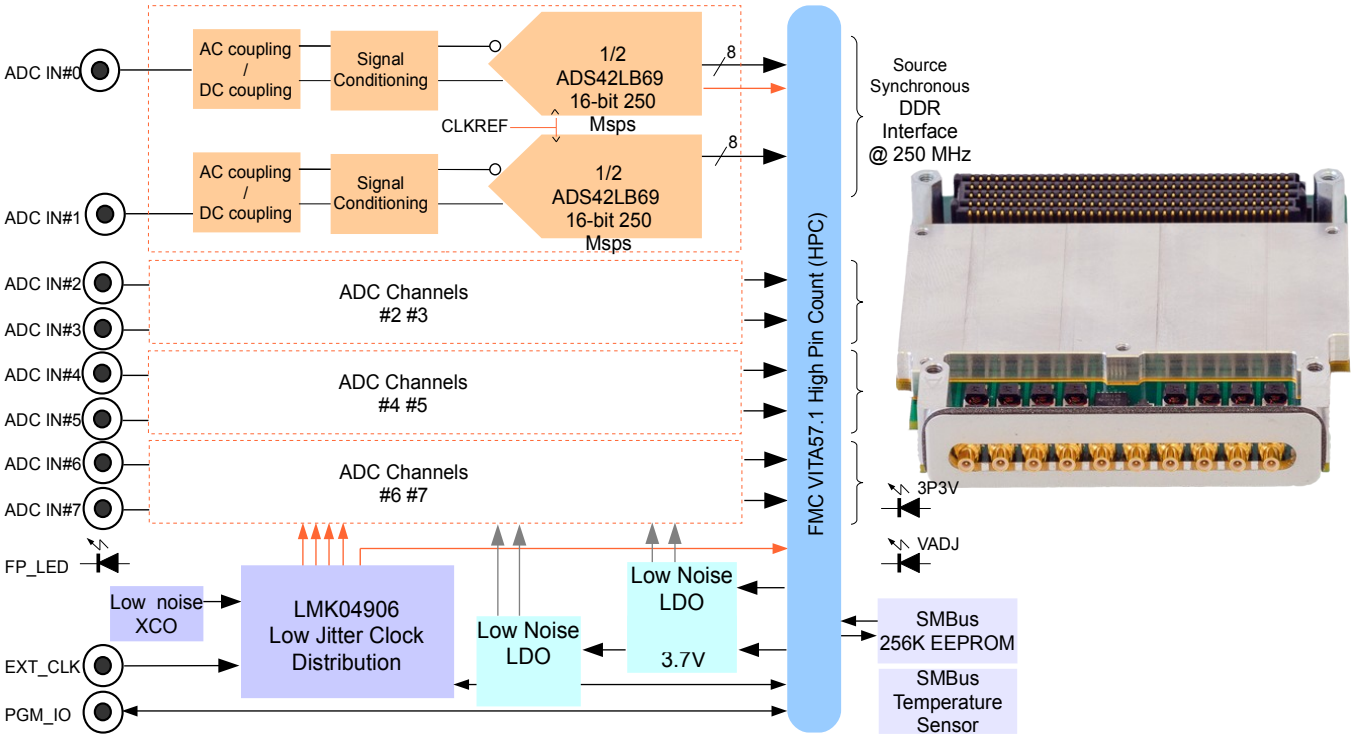
ADC_3110/3111 – Eight Channel 16-bit ADC

FMC Mezzanine Board

Data Sheet
ADC_3110_DS_A0



Key Features

- Eight channel (8) 16-bit/250Msps ADC
- Single width FMC VITA 57.1-2008
  - HPC 400 pins connector
  - Ten(10) SSMC front panel connectors
  - 8[W] typical power consumption
  - FMC 12[V] power supply not required
  - LVDS high speed interface
- Based on latest generation ADC technology
  - TI ADS42LB69 dual 16-bit/250 Msps
  - Single ended AC coupling (ADC_3110)
  - Single ended DC coupling (ADC_3111)
  - High-speed LVDS data read-out
- Sophisticated clock tree distribution
  - TI LMK4906 (dual PLL)
  - On-board ultra-low noise oscillator /VCXO
  - External SSMC Clock reference
- On board low noise power supplies generation
  - FMC 12P0V power supply not used
- Temperature sensor monitoring through SMBus
- XILINX Virtex 6/7 FPGA VHDL Design Kit
- LINUX Software Library
- Direct EPICS support on IFC_1210 carrier

Overview

IOxOS Technologies introduces the ADC_3110/3111, a VITA 57.1-2008 standard eight (8) channels 16-bit 250 Msps ADC.

The ADC_3110/3111 is the 1st member of a FMC family products which includes high speed DAC, GSPS ADC 10/12 bits and programmable digital IO.

The eight(8) single-ended analog inputs are supplied through SSMC high frequency connectors. AC coupling (ADC_3110) and DC coupling (ADC_3111) versions are available.

Three (3) AC coupling input conditioner schema is also available for optimal target application.

Clock tree is implemented with a high precision on-board low jitter low phase noise clock controller LMK04906 fully programmable by the carrier-board. The clock reference source is selectable from front panel SSMC input or from an on-board ultra-low phase noise XCO/VCXO.

A user programmable LVTTL GPIO SSMB can be defined as TRIGGER, GATE, CLOCK replication or any user defined function.

The ADC_3110/3111 targets the following applications:

- Test measurement equipments
- Radar/Sonar
- Scientific / Physics experiments

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Introduction

IOxOS Technologies introduces the ADC_3110/3111, a FMC VITA57.1 module featuring a high density ADC 16-bit/250Msps based on latest generation TI ADC ADS42LB69.

AC coupling front-end (ADC_3110)

The ADC_3110 AC coupling input schema can be optionally selected for optimal fit to the targeted application.

- Dual BALUN Mini-Circuits TC1-1-13MX+ (default)
- Single BALUN Mini-Circuits TC1-1X+

DC coupling front-end (ADC_3111)

The ADC_3111 implements DC coupling input stage built with ultrahigh dynamic range differential amplifier ADL5565. The DC input common mode offset is programmable through on-board 16-bit DAC from - 1.0[V] to +1.0[V].

Clock Distribution

The on-board clock distribution is implemented with a low-noise low-jitter dual PLL clock driver TI LMK04906. The input clock source can be selected from :

- Front panel AC coupled SSMC “CLKREF”
- On-board ultra-low phase noise oscillator (Crystek CCHD-575)
- Front panel AC coupled SSMC “CLKREF” with ultra-low phase noise VCXO

Five(5) output clocks, with programmable delay in steps of 25ps, are supplied to the four(4) ADS42LB69 devices and to the FMC CLK0_M2C.

The LMK04906 incorporates a uWIRE Bus and is fully programmable from the carrier board FPGA.

Power Supplies

The ADC_3110/3111 on-board power supplies are built locally with low noise devices.

A bulk DCDC generates a local 3.8[V] from the FMC P3V3 power supply. (FMC P12V0 is not used). This local 3.8[V] is used as source for three LDO generating :

- Low noise 3.3[V] for ADS42LB69 devices
- Low noise 1.8[V] for ADS42LB69 devices
- Low noise 3.3[V] for LMK04906 + CCHD-575/VCXO

The DCDC operating frequency can be synchronized by the carrier board.

One low noise LDO is directly powered by FMC VADJ and generates a local 1.8[V] dedicated to ADS42LB69 digital read-out section (LVDS).

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Other Resources

The ADC_3110 also includes two SMBus connected devices

- EEPROM 256K
- Temperature sensor TMP102 located on middle of the ADS42LB69 PCB layout implementation

FPGA Design Kit

A FPGA Design Kit, is available in VHDL format for XILINX Virtex-6(7), providing complete FMC_3110/3111 carrier FPGA interface, together with:

- General DAQ Management
- ADS42LB69 Data Acquisition in embedded DPRAM
- SPI Bus controller for ADS42LB69
- uWIRE Bus controller for LMK04906
- GPIO, LED, and basic control functions

Firmware/Software Support

A complete IFC_1210 TOSCA II environment including FPGA firmware (source and binary files) and LINUX libraries with examples is also available.

This distribution kit allows to manage at OS level a IFC_1210 system based on ADC_3110/3111 with application example.

An EPICS Driver for TOSCA II infrastructure is also available. EPICS drivers for IFC_1210 were developed by PSI and provided as Open-Source upon request, under an Open-Source license from PSI (http://controls.web.psi.ch).

IOxOS Technologies also provides design services for the development of application specific VHDL for XILINX and ALTERA platforms.

ENOB, SNR, SFDR Performance

Consult IOxOS Technologies
For up to date data

Ordering Information

Article Reference	*Product Description*
ADC_3110-A0	AC coupling version (dual TC1-1-13MX+)
ADC_3110-A1	AC coupling version (single TC1-1X+)
ADC_3110-A2	AC coupling version (dual TC1-1-13MX+) with on-board VCXO
ADC_3111-A0	DC coupling version
FDK_3110	FPGA VHDL Design reference kit

For other configurations please contact IOxOS Technologies